Notice of Allowability	Application No.	Applicant(s)	
	10/785,166	NEMATI ET AL.	
	Examiner	Art Unit	
	William C. Vesperman	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *2/23/2004*.

2. ☒ The allowed claim(s) is/are *1-3*.

3. ☒ The drawings filed on *23 February 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 2/23/2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Carl Whitehead

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Detailed Action

1. This action is in reply to applicant's reply of 2/23/2004.

Allowed Subject Matter

2. Claims 1 – 3 are allowed.

3. The following is a statement of reasons for the indication of allowable subject matter.

Hsu et al. (US 2002/0190265) teaches a method for manufacturing a thyristor-based semiconductor device having a substrate and a thyristor body region therein, the method comprising: forming a doped layer over the substrate, forming a nitride layer over the doped layer; forming an oxide layer over the nitride layer; etching a trench in nitride and oxide layers, the trench having a bottom adjacent to a doped layer; and forming a thyristor body region in the trench adjacent to and in between two separate transistors.

The prior art does not teach or suggest, in combination with the other claimed limitations, a method for manufacturing a thyristor-based semiconductor device having a substrate and a thyristor body region therein, the method comprising: etching a trench in the substrate and adjacent to the thyristor body region, the trench having a bottom; implanting a portion of the thyristor body region and a first portion of the substrate that is adjacent to the bottom of the trench with a first dopant at a first implant energy, thereby forming a first doped well region and a first base region of the thyristor body region; annealing the first doped well region; implanting a first thyristor emitter region in the first

doped well region and contiguously adjacent to the first base region, the first thyristor emitter region being of a polarity that is opposite the polarity of the first doped well region, the first doped well region being susceptible to carrier accumulation via carrier drainage from the first thyristor emitter region; forming a carrier coupler electrically coupled to the first doped well region, the carrier coupler being configured and arranged to drain carriers accumulated in the first doped well region; and forming a control port in the trench and adapted to capacitively couple to the thyristor body and to control current in the thyristor body.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Horch et al. (US 6,767,770) teaches a self aligned thyristor structure.

Noble et al. (US 6,545,297) teaches a SRAM cell with latch-up.

Cho et al. (US 6,583,452) teaches a thyristor based device with capacitive coupling.

Harari (US 4,395,723) teaches a floating substrate dynamic RAM cell.

Malhi et al. (US 4,797,373) teaches a DRAM cell with a trench capacitor.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Vesperman whose telephone number is 571-272-1701. The examiner can normally be reached on Mon. - Fri., 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WCV

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November 1, 2004